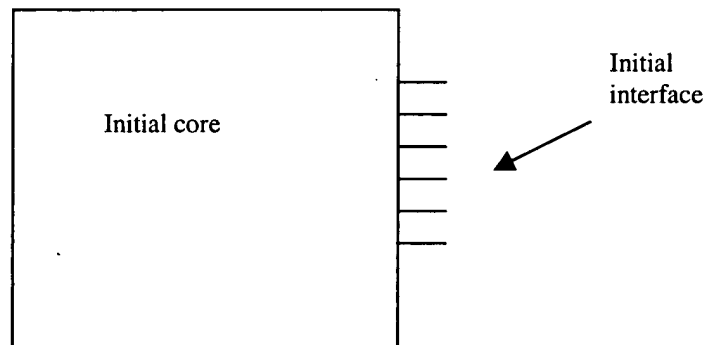
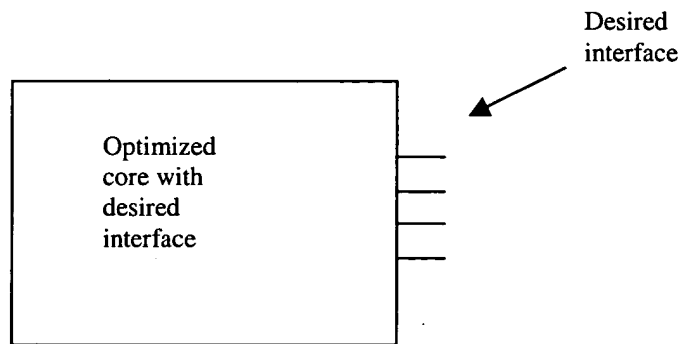


**Figure 1a: Initial core (Prior Art)**



**Figure 1b: Core with re-designed Interface (Prior Art)**



**Figure 1c: Core of 1.a with external interface logic (Prior Art)**

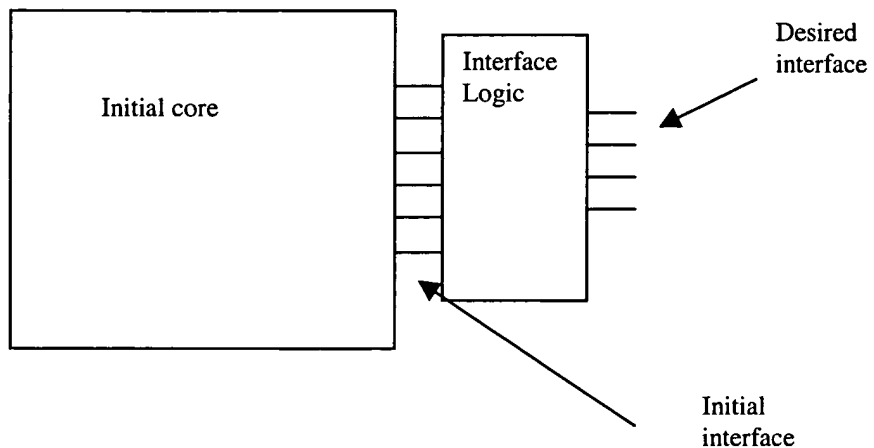


Figure 2a:

Name	Signal width	Function
Clk	1	Clock
MCmd	2	Command
MAddress	32	Address
Mdata	64	Write Data
SCmdAccept	1	Accept Command
SResp	2	Response
SData	64	Read Data

Figure 2b:

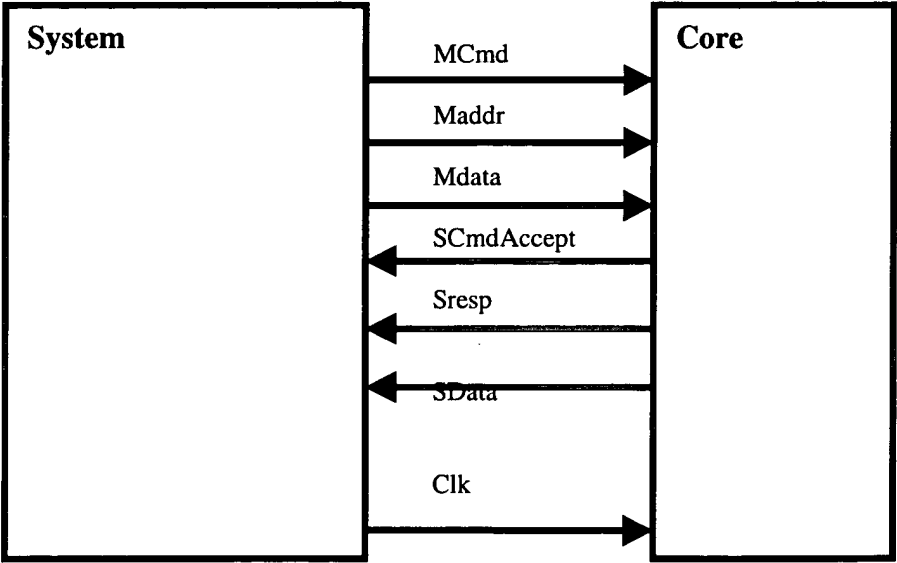


Figure 3a:

Command encoding	Function
00	Idle command
01	Read Command
10	Write Command
11	Exclusive Read Command

Figure 3b:

Burst encoding	Burst Function
000	Incrementing burst with burst length of 1
001	Incrementing burst with burst length of 2
010	Incrementing burst with burst length of 4
011	Incrementing burst with burst length of 8
100	Non-Incrementing burst

000000"5404E960

Burst encoding	Burst Function
000	Incrementing burst with burst length of 1
001	Incrementing burst with burst length of 2
010	Incrementing burst with burst length of 4
011	Incrementing burst with burst length of 8
100	Non-Incrementing burst

Figure 3c

Figure 4:

Signal Name	Width	Parametrization	Signal Enabling	Function
Clk	1	N	N	Clock
Reset	1	N	Y	Reset
MCmd	2	N	N	Request Command
MAddr	1-32	Y	N	Request Address
MData	8:16:32:64	Y	N	Request Write Data
MBurst	3	N	Y	Request Burst
MByteEn	1:2:4:8	Y	Y	Request Byte Enable
MDataValid	1	N	Y	Write Data Valid
SCmdAccept	1	N	N	Accept Command
SDataAccept	1	N	With MDataValid	Accept Write Data
SResp	2	N	N	Response
SData	8:16:32:64	Y	N	Read Response Data
MFlag	1:8	Y	Y	Master Out of Band signal
SFlag	1:8	Y	Y	Slave Out of Band Signal
MError	1	N	Y	Master Error
SError	1	N	Y	Slave Error

00000"5404E960

**Figure 5:**

MData_WIDTH	16	
MAddr_WIDTH		32
MBurst_ENABLE	1	
MByteEn_ENABLE	1	
MByteEn_WIDTH	4	
MDataValid_ENABLE	0	
MFlag_ENABLE	1	
MFlag_WIDTH	2	
SFlag_ENABLE	0	
MError_ENABLE	1	
SError_ENABLE	0	

00000000 "5404E3E0"

Figure 6:

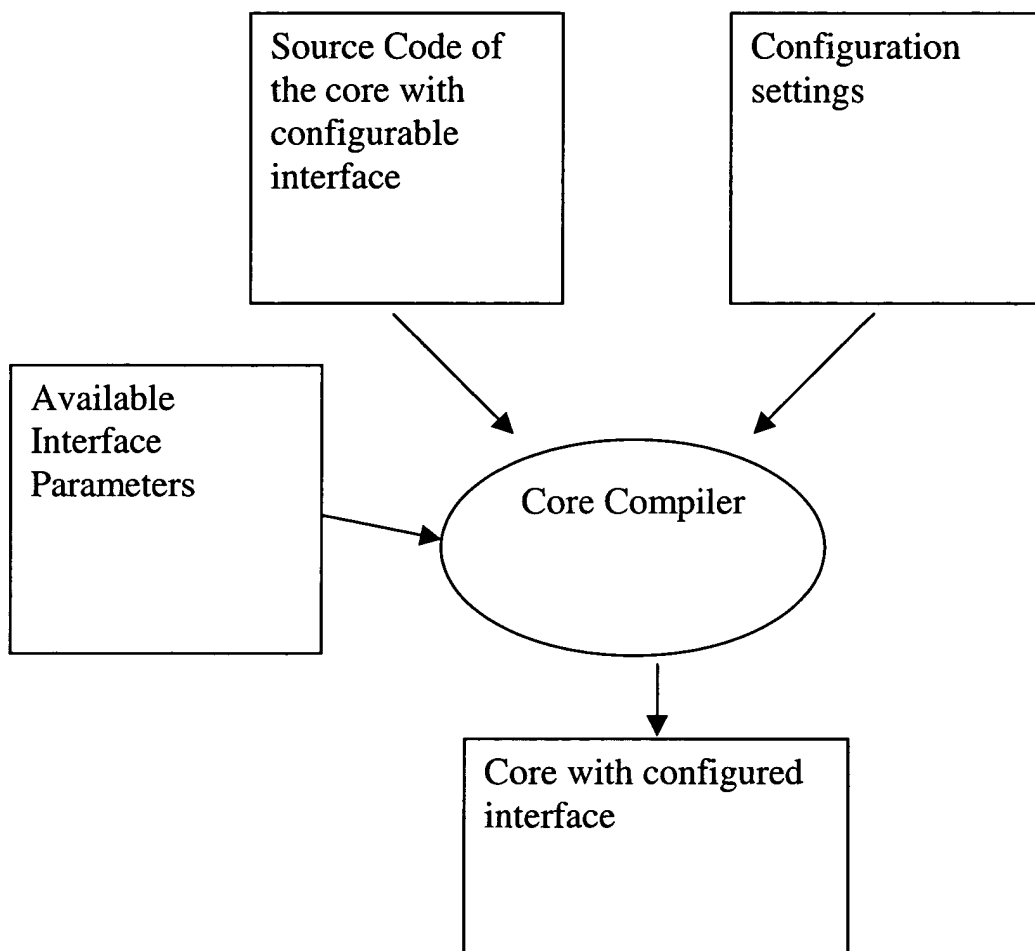


Figure 7:

**Configure Open Core Protocol**

Connection Name:  Address Width:  Data Width:

Simple Extensions	Sideband Extensions	Thread Extensions	Control and Status
<input type="checkbox"/> Burst Mode	<input checked="" type="checkbox"/> Reset	<input checked="" type="checkbox"/> Use Threads	<input checked="" type="checkbox"/> Use Control Information
<input type="checkbox"/> Data Handshake	<input type="checkbox"/> Slave Interrupt	Thread Width: <input type="text" value="2"/>	<input type="checkbox"/> Control Write Event
<input type="checkbox"/> Response Accept	<input type="checkbox"/> Slave Error	<input type="checkbox"/> Use Connections	<input type="checkbox"/> Control Busy Event
<input checked="" type="checkbox"/> Words Only	<input checked="" type="checkbox"/> Use Master Flag	Connection Width: <input type="text" value="4"/>	Control Field Width: <input type="text" value="1"/>
<input checked="" type="checkbox"/> General Byte Enable	Master Flag Width: <input type="text" value="3"/>	<input type="checkbox"/> Data Thread Id	<input checked="" type="checkbox"/> Use Status Information
<input checked="" type="checkbox"/> Aligned Byte Enable	<input checked="" type="checkbox"/> Use Slave Flag	<input type="checkbox"/> Master Thread Busy	<input type="checkbox"/> Status Read Event
	Slave Flag Width: <input type="text" value="4"/>	<input type="checkbox"/> Slave Thread Busy	Status Field Width: <input type="text" value="1"/>

008080" 5404E960